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PTO/SB/08A (08-00)

Substitute for form 1449A/PTO		<i>Complete if Known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	09/994,592
		Filing Date	November 27, 2001
		First Named Inventor	Raghavan MENON et al.
		Group Art Unit	2661
		Examiner Name	Unassigned
Sheet	1	of	1
		Attorney Docket Number	VIVC001/00US

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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code ² (if known)		

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)			

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
PO	1	Ed. by T. G. ROBERTAZZI, "Performance Evaluation of High Speed Switching Fabrics and Networks: ATM, Broadband ISDN, and MAN Technology", IEEE Press, ISBN 0-7803-0436-5, pp. 1-467.	
PO	2	C. ROSE et al., "The Performance of Random and Optimal Scheduling in a Time-Multiplex Switch," IEEE Transactions on Communications, Vol. COM-35, No. 8, August 1987, pp. 813-817.	
PO	3	T. ANDERSON, et al. "High-Speed Switch Scheduling for Local-Area Networks," ACM Transactions on Computer Systems, Vol. 11, No. 4, Nov. 1993, pp. 319-352	

Examiner Signature		Date Considered	11/14/05
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- ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
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		Number	Kind Code ² <i>(if known)</i>		
PO		6,157,957		Berthaud	12-05-2000
PO		6,101,599		Wright, et al.	08-08-2000
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FOREIGN PATENT DOCUMENTS							
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		Office ³	Number ⁴	Kind Code ⁵ <i>(if known)</i>			
PO			WO 00/64109		Hughes et al.	10-26-2000	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁷
PO		N. MCKEOWN, "The iSLIP Scheduling Algorithm for Input-Queued Switches", <i>IEEE Transactions on Networking</i> , Vol. 7, No. 2, April 1999, 22 pages.	
PO		N. MCKEOWN, et al., "The Tiny Tera: A Packet Switch Core", <i>Hot Interconnects V, Stanford University</i> , August 1996.	
PO		K. Y. K. CHANG et al., "A 50 Gb/s 32 x 32 CMOS Crossbar Chip using Asymmetric Serial Links", <i>1999 Symposium on VLSI Circuits, Digest of Technical Papers</i> , 4 pages.	
PO		K. Y. K. CHANG et al., "A 2 Gb/s Asymmetric Serial Link for High-Bandwidth Packet Switches", <i>Hot Interconnects VI, pp. 171-179, Stanford University, August 1997</i> , 9 pages.	
PO		N. UZUN et al., "Ten Terabit Multicast Packet Switch with SRRM Scheduling Algorithm", <i>New Jersey Institute of Technology</i> , pp. 1-10, 1999.	
PO		N. MCKEOWN, "Scheduling Algorithms for Input-Queued Cell Switches", pp. 1-119, Ph.D. Thesis, University of California at Berkeley, May 1995.	

Examiner Signature	<i>Dorell Jan</i>	Date Considered	11/15/05
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